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substitutions, and alterations without departing from the spirit and scope of the invention.

What is claimed is:

1. A method, comprising:

receiving a source SRAM cell having at least two pull-up transistors, at least two pull-down transistors, and at least pass gate transistors, each of the transistors having a drawn size, each of the transistors being a conventional MOS transistor:

generating a target SRAM cell by replacing one or more of the conventional MOS transistors in the received SRAM cell with a replacement transistor having a reduced threshold voltage variation as compared to the corresponding conventional transistor, the replacement transistor having a drawn gate size that is substantially identical to that of the corresponding conventional transistor;

determining base minimum supply voltage and a corresponding base failure rate of the conventional SRAM cell, the base minimum supply voltage being a lowest 20 supply voltage at which a predetermined percentage of the SRAM cells can correctly perform read and write operations, the failure rate corresponding to the percentage of SRAM cells that fail at the base minimum supply voltage; 25

determining at least one base threshold voltage (Vt) of at least one transistor in the target SRAM cell, and a base supply voltage for the target SRAM cell; and

modifying the target SRAM cell to generate a target SRAM cell having a lower base minimum supply voltage, the 30 steps for modifying further comprising:

(i) determining one or more candidate failure rates of a group of the target SRAM cells in response to one or more modified threshold voltage candidate values of the at least one transistor, the candidate failure rates being determined for the base 35 minimum power supply voltage;

if the failure rate for one of the modified threshold voltage values is lower than the base failure rate, saving the one modified threshold voltage candidate value as the base threshold voltage value and returning to (i);

if the failure rate for one of more of the modified threshold voltage values is not lower than the base failure rate, but is lower than a predetermined target failure rate, reducing the base minimum supply voltage by a predetermined voltage step, and returning to (i); and

if the failure rate for one or more of the modified threshold voltage candidate values is greater than a failure limit, saving the current threshold voltage value and base minimum power supply voltage as target features of the target SRAM cell.

2. The method of claim 1, wherein:

determining the one or more candidate failure rates of the group of the target SRAM cells includes determining the failure rate for SRAM cells with cross-coupled transistor pairs having screening regions formed below their 55 channels, the screening regions being doped to a conductivity type opposite to their source-drains, and to a dopant concentration of no less than 1×10¹⁸ dopant atoms/cm³.

3. The method of claim 1, wherein:

determining the at least one base Vt of at least one transistor in the target SRAM cell, includes determining a base n-channel Vt (Vtn) and a base p-channel Vt (Vtp) for transistors of the SRAM cells.

4. The method of claim 1, wherein:

determining one or more candidate failure rates of a group of the target SRAM cells comprises:

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establishing at least a first threshold voltage change $\Delta V t, \\$ and

determining one or more failure rate corresponding to the threshold voltages values of Vtn+ Δ Vt, Vtp and Vtn- Δ Vtn, Vtp; wherein

Vtn is a base n-channel Vt and Vtp is a base p-channel Vt.

5. The method of claim 4, wherein:

determining a failure rate of a group of the SRAM cells further includes determining one or more candidate failure rates for the threshold voltage values of Vtn, Vtp+ $\Delta Vt;$ Vtn, Vtp- $\Delta Vtn,$ Vtp+ $\Delta Vt,$ Vtn+ $\Delta Vt,$ Vtp+ $\Delta Vt,$ Vtn+ $\Delta Vt,$ Vtp- $\Delta Vt,$ Vtp-

6. The method of claim **4**, wherein:

generating a target SRAM cell by replacing one or more transistors in an existing SRAM cell with a replacement transistor having a same gate size but reduced threshold voltage variation as compared to the replaced transistor,

determining base supply voltage for a base failure rate of the conventional SRAM cell, the base supply voltage being a lowest supply voltage at which the existing SRAM cells have the base failure rate;

determining at least one base threshold voltage (Vt) of at least one transistor in the target SRAM cell; and

modifying the target SRAM cell to generate a target SRAM cell having a lower base minimum supply voltage, comprising:

(i) modifying the Vt of at least one transistor in target SRAM cells from the base Vt, and determining a failure rate of the target SRAM cells at a current base supply voltage;

if the failure rate for the modified Vt is lower than the base failure rate, saving the modified Vt as the base Vt and returning to (i);

if the failure rate for the modified Vt is not lower than the base failure rate, but is lower than a maximum failure rate, reducing the base supply voltage by a predetermined voltage step, and returning to (i); and

if the failure rate for the modified Vt is greater than the maximum failure limit, saving the current threshold voltage value and base minimum power supply voltage as target features of the target SRAM cell.

7. The method of claim 6, wherein:

determining the failure rates of target SRAM cells includes determining the failure rate for SRAM cells with cross-coupled transistor pairs having screening regions formed below their channels, the screening regions being doped to a conductivity type opposite to their source-drains, and to a dopant concentration of no less than 1×10¹⁸ dopant atoms/cm³.

8. The method of claim 7, wherein:

the cross-coupled transistors further include undoped channel regions having a dopant concentration of no more than 1×10¹⁷ dopant atoms/cm³.

9. The method of claim 6, wherein:

determining at least one base Vt of at least one transistor in the target SRAM cell includes determining a base n-channel Vt (Vtn) and a base p-channel Vt (Vtp) for transistors of the SRAM cells.

10. The method of claim 6, wherein:

modifying the Vt of at least one transistor in the target SRAM cells from the base Vt includes changing a body bias voltage of the at least one transistors.

11. The method of claim 1, wherein:

determining the failure rates of target SRAM cells includes.

establishing at least a first threshold voltage change ΔVt , and

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